INFORMATION DISCLOSURE CITATION

(Use several sheets if necessary)

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Docket Number (Optional)	Application Number
BUR920010192US1	10/063427
Applicant(s) Mitchell DeHond, et al.	
Filing Date 04/23/02	**Group Art Unit**

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL	REF	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
BB		3,751,647	08/07/73	Maeder, et al.			
BB		5,084,824	01/28/92	Lam, et al.			
BB		5,438,527	08/01/95	Feldbaumer, et al.			
BB		5,539,652	07/23/96	Tegethoff			
BB		5,754,826	05/19/98	Gamal, et al.			
BB		5,773,315	06/30/98	Jarvis			
BB		5,953,518	09/14/99	Sugasawara, et al.			
BB		6,044,208	03/28/00	Papadopoulou, et al.			
BB		6,070,004	05/30/00	Prein			
BB		6,169,960	01/02/01	Ehrichs			
BB		6,210,983	04/03/01	Atchison, et al.			

FOREIGN PATENT DOCUMENTS

	REF	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation YES	Translation NO
BB		JP6216249	08/05/94	Japan				
BB		JP1024225	09/11/98	Japan				

OTHER DOCUMENTS *(Including Author, Title, Date, Pertinent Pages, Etc.)*

BB		Michael Retersdorf, "Yield Focused Defect Reduction Methodology", 3/99, IEEE/SEMI Advanced Semiconductor Manufacturing Conference, pp. 309 - 313
BB		K.W. Lallier and A.D. Savkar, "Relating Logic Design to Physical Geometry in LSI Chip", IBM Technical Disclosure Bulletin, Vol. 19 No. 6, November 1976, pp. 2140-2143.

EXAMINER	DATE CONSIDERED
Brian Bowman	3/5/04

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP Section 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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U.S. PATENT DOCUMENTS

*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
BB		6,305,004	10/16/01	Tellez, et al.	1	1	
BB		6,311,139	10/30/01	Kuroda, et al.	1	1	

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES	TRANSLATION NO

OTHER DOCUMENTS *(Including Author, Title, Date, Pertinent Pages, Etc.)*

BB			C.H. Stapper, "High Yield Semiconductor Logic Wiring", Vol. 30 No. 11 April 1988, IBM Technical Disclosure Bulletin, pp. 366-367.
BB			D.Guedj and M. Rivier, "Method to Computer the Random Photo Yield of Integrated Circuits", Vol. 32, No. 7, December 1989, IBM Technical Disclosure Bulletin, pp. 242 - 244.

EXAMINER	DATE C NSIDERED
Brian Johnson	3/5/04

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